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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/010,819	12/06/2001	John Lawrence Melanson	1064-CA	7277

31127 7590 06/01/2005

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EXAMINER	
WANG, TED M	

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 06/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/010,819	MELANSON, JOHN LAWRENCE	
	Examiner	Art Unit	
	Ted M. Wang	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 14-20* is/are rejected.

7)☒ Claim(s) *10-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

- On paragraph 32, line 2 and line 8, change "603" to --- 604 ---, respectively.
- On paragraph 35, line 8, change "804" to --- 704 --- after "capacitors" and change "804" to --- 705 --- after "amplifiers".
- On paragraph 35, line 13, change "800" to --- 700 ---.
- On paragraph 37, line 9, change "805" to --- 807 ---.

Appropriate correction is required.

Claim Objections

2. Claims 3 and 20 are objected to because of the following informalities:

- In claim 3, line 1, change "2" to --- 1 ---.
- In claims 20, line 1, insert --- 16 --- after "Claim".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 4-9, 14-16, and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Corry et al. (US 5,563,535) in view of Dairi (US 6,515,526).

- With regard claim 1, Corry et al. discloses a clock generator comprising:

  input circuitry (Fig.1 element 101 and Fig.2 element 201) for receiving an input signal and a clock (Fig.1 element 101 clock input and Fig.2 element 201 clock input) generating a memory address therefrom (Fig.1 element 103, Fig.2 element 207 input, m, column 1, line 28 – column 2, line 46 and column 5, lines 10-38);

  a memory (Fig.1 element 103, Fig.2 element 207, column 1, lines 28-35, and column 5, lines 10-38) for storing digital data indexed by said memory address (column 1, line 28 – column 2, line 46 and column 5, lines 10-38) and representing at least a portion of a substantially sinusoidal analog clock (column 2, lines 7-19 and column 4, lines 48-62);

  a digital to analog converter for converting data retrieved from said memory to generate said analog clock (Fig.1 element 109 and Fig.2 element 209);

  a filter for filtering the substantially sinusoidal analog clock (Fig.2 element 217 and column 5, lines 39-45).

  Corry et al. discloses all of the subject matter as described in the above paragraph except for specifically teaching a circuitry for converting the substantially sinusoidal analog clock to a digital output clock.

  However, Dairi teaches a circuitry for converting the substantially sinusoidal analog clock to a digital output clock (Fig.1 elements 2-6 and Fig.3 element 6).

It is desirable to include a circuitry for converting the substantially sinusoidal analog clock to a digital output clock in order to improve the phase fluctuation without being limited to the comparison frequency range in phase detection (column 7, lines 43-47). Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include the apparatus as taught by Dairi in which, including a circuitry for converting the substantially sinusoidal analog clock to a digital output clock, into Corrys' DDS clock circuit so as to improve the phase fluctuation without being limited to the comparison frequency range in phase detection.

- With claim 2, Corry et al. further discloses a bandpass filter (Fig.2 element 217).
- With claim 4, Corry et al. further discloses that the memory stores digital data representing real and imaginary parts of a complex waveform (Fig.4 elements 207 and 401 and column 6, lines 45-62).
- With claim 5, all limitation is contained in claims 4 and 2. The explanation of all the limitation is already addressed in the above paragraph.
- With claim 6, Corry et al. discloses all of the subject matter as described in the above paragraph except for specifically teaching that the circuitry for converting comprises a comparator.

  However, Dairi teaches that the circuitry for converting comprises a comparator (Fig.1 element 2).

  It is desirable that the circuitry for converting comprises a comparator in order to improve the frequency stability. Therefore, It would have been obvious to one of

ordinary skill in the art at the time of the invention was made to include the apparatus as taught by Dairi in which, including the circuitry for converting comprises a comparator, into Corrys' DDS clock circuit so as to improve the frequency stability.

- With claim 7, all limitation is contained in claim 1. The explanation of all the limitation is already addressed in the above paragraph.
- With claim 8, Corry et al. further discloses that the input circuitry comprises a phase-frequency detector (Fig.1 element 101 and Fig.2 element 201) comparing the input signal with a reference (Fig.1 element 101 clock input and Fig.2 element 201 clock input); and

  a delta - sigma noise shaper for filtering at least a selected number of data bits output (Fig.2 element 203 and column 5, lines 10-37) from said phase-frequency detector to generate selected bits of said memory address (column 1, line 28 – column 2, line 46 and column 5, lines 10-38).
- With regard claim 9, all limitation is contained in claims 7 and 8. The explanation of all the limitation is already addressed in the above paragraph.
- With claim 14, Corry et al. further discloses a delta sigma converter (Fig.2 element 203). All other limitation is contained in claim 9. The explanation of all the limitation is already addressed in the above paragraph.
- With claim 15, Corry et al. further discloses that circuitry for generating a memory index comprises a noise shaper for shaping noise output (Fig.2 element 203 and

column 5, lines 10-37) from said phase detector (Fig.1b element 115, and column 2 lines 7-46) to reduce a size of said memory.

- With regard claim 16, which is a system claim related to claim 1, all limitation is contained in claim 1. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 18, which is a system claim related to claim 4, all limitation is contained in claim 4. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 19, which is a system claim related to claim 2, all limitation is contained in claim 2. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 20, which is a system claim related to claim 7, all limitation is contained in claim 7. The explanation of all the limitation is already addressed in the above paragraph.

5. Claims 3 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Corry et al. (US 5,563,535) and Dairi (US 6,515,526) as applied to claim 1 above, and further in view of Sheffer et al. (US 4,951,004).

- With regard claim 3, Corry et al. and Dairi disclose all of the subject matter as described in the above paragraph except for specifically teaching a low pass filter after digital to analog converter.

  However, Sheffer et al. teaches a low pass filter after digital to analog converter in a DDS circuit (Fig.1 element LPF and column 1, lines 63-68).

It is desirable to include a low pass filter after digital to analog converter in a DDS circuit in order to improve the clock signal noise by removing the spurious frequency component higher that the Nyquist frequency (column 1, lines 63-68). Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include the apparatus as taught by Sheffer et al. to replace the band pass filter with a low pass filter into Corry et al. and Dairis' modified DDS circuit so as to improve the clock signal noise by removing the spurious frequency component higher that the Nyquist frequency.

- With regard claim 17, which is a system claim related to claim 3, all limitation is contained in claim 3. The explanation of all the limitation is already addressed in the above paragraph.

Allowable Subject Matter

6. Claims 10-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. Reference(s) US 6,075,474 and US 6,483,388 are cited because they are put pertinent to the DSS using Sigma-Delta modulation. However, none of references teach detailed connection as recited in claim.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted M. Wang whose telephone number is 571-272-3053. The examiner can normally be reached on M-F, 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 571-272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ted M Wang
Examiner
Art Unit 2634

Ted M. Wang

SHUWANG LIU
PRIMARY EXAMINER